WHAT IS CLAIMED IS:

1. A method of using a CMOS sensor array to perform a spatial to frequency transform of analog signals from sensor elements of said array, said transform being characterized by a basis function, comprising the steps of:

applying a pulsewidth modulated wordline signal to at least one sensor element of said array;

applying a pulsewidth modulated bitline signal to said at least one sensor element;

wherein the coincidence of said pulsewidths has a duration corresponding to a product of coefficients of said basis function;

accumulating the current from said at least one sensor element during said coincidence; and

repeating said applying and accumulating steps as required by said transform.

2. The method of Claim 1, wherein said basis function corresponds to a discrete cosine transform.

3. The method of Claim 1, wherein said step of accumulating charge is performed for a positive and negative output of said sensor element.

4. The method of Claim 1, wherein said transform is performed on blocks of sensor elements and said steps of applying pulses are performed for all wordlines of a block and all bitlines of said array simultaneously.

5. The method of Claim 1, wherein said applying steps are performed with pulsewidths that correspond to separable coefficients of said basis function.

6. The method of Claim 1, wherein said step of applying a pulsewidth modulated bitline signal is performed with repeated pulses of said bitline signal.

7. A method of providing pulsewidth modulated bitline and wordline signals for performing spatial to frequency transforms of analog signals from sensor elements of a CMOS sensor array, said transform being characterized by a basis function, comprising the steps of:

dividing a wordline period into intervals, such that each interval has an accumulated pulsewidth corresponding to a coefficient of said basis function, thereby providing a pulsewidth modulated wordline signal; and

dividing a bitline period into said intervals and into subintervals, such that each subinterval of each interval has an accumulated pulsewidth corresponding to a coefficient of said basis function.

8. The method of Claim 7, wherein said transform is a discrete cosine transform.

9. The method of Claim 7, wherein said transform is a discrete articulated trapezoid transform.

10. An integrated circuit for acquiring images and performing a spatial to frequency transform of analog signals representing said image, comprising:

a CMOS sensor array, having rows and columns of sensor elements, each row of sensor elements having an associated wordline and each column of sensor elements having an associated bitline;

wordline driver circuitry operable to provide wordline activation signals on said wordlines;

bitline driver circuitry operable to provide bitline activation signals on said bitlines;

column circuitry operable to accumulate current from said columns; and

a pulsewidth timing unit for controlling pulse widths of said wordline activation signals and said bitline activation signals.

11. The circuit of Claim 10, wherein each said bitline is bifurcated so as to provide a positive and a negative output.

12. The circuit of Claim 10, further comprising comparators operable to determine whether said current exceeds a predetermined threshold.

13. The circuit of Claim 10, further comprising analog-to-digital converters operable to convert said current to a digital value.

14. An integrated circuit for acquiring images and performing a spatial to frequency transform of analog signals representing said image, said transform being characterized by a basis function, comprising:

a CMOS sensor array, having rows and columns of sensor elements, each row of sensor elements having an associated wordline and each column of sensor elements having an associated bitline;

wordline driver circuitry operable to provide wordline activation signals on said wordlines;

bitline driver circuitry operable to provide bitline activation signals on said bitlines;

column circuitry operable to accumulate current from said columns;

comparators operable to compare analog output signals of said column circuitry with threshold values; and

analog-to-digital converters operable to convert above-threshold outputs of said comparators to digital values.

15. The circuit of Claim 14, wherein said analog-to-digital converters incorporate a quantization scheme.

16. The circuit of Claim 14, further comprising encoding circuitry operable to encode outputs of said analog-to-digital converters.